



Performance Tuning PCIe® Systems

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Disclaimer



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Agenda



- **Performance Tuning**
- **Replay Buffer**
- **Credits**
- **Posted Requests**
- **Non Posted Requests**
- **Performance Measurement**
- **Examples**

Performance Tuning

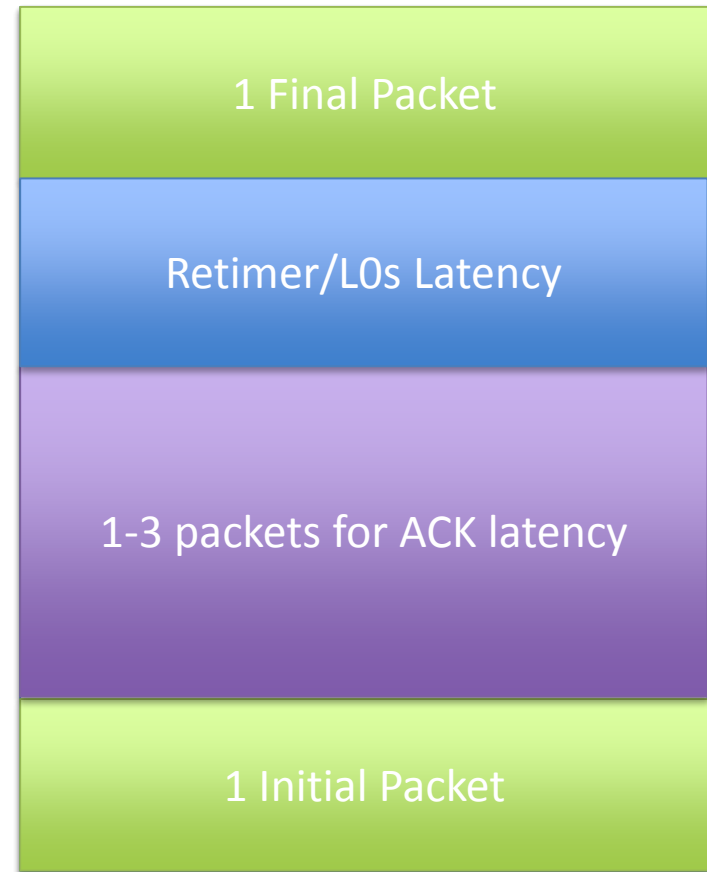


- **Link Width (x1-x16)**
- **Maximum Speed (2.5GT/s - 16 GT/s)**
- **Adjustments**
 - Replay Buffer Sizing
 - Credits
 - Tags and Payload/Request Sizes
- **Measurement**
 - Simulation Environment

Retry Buffer Sizing

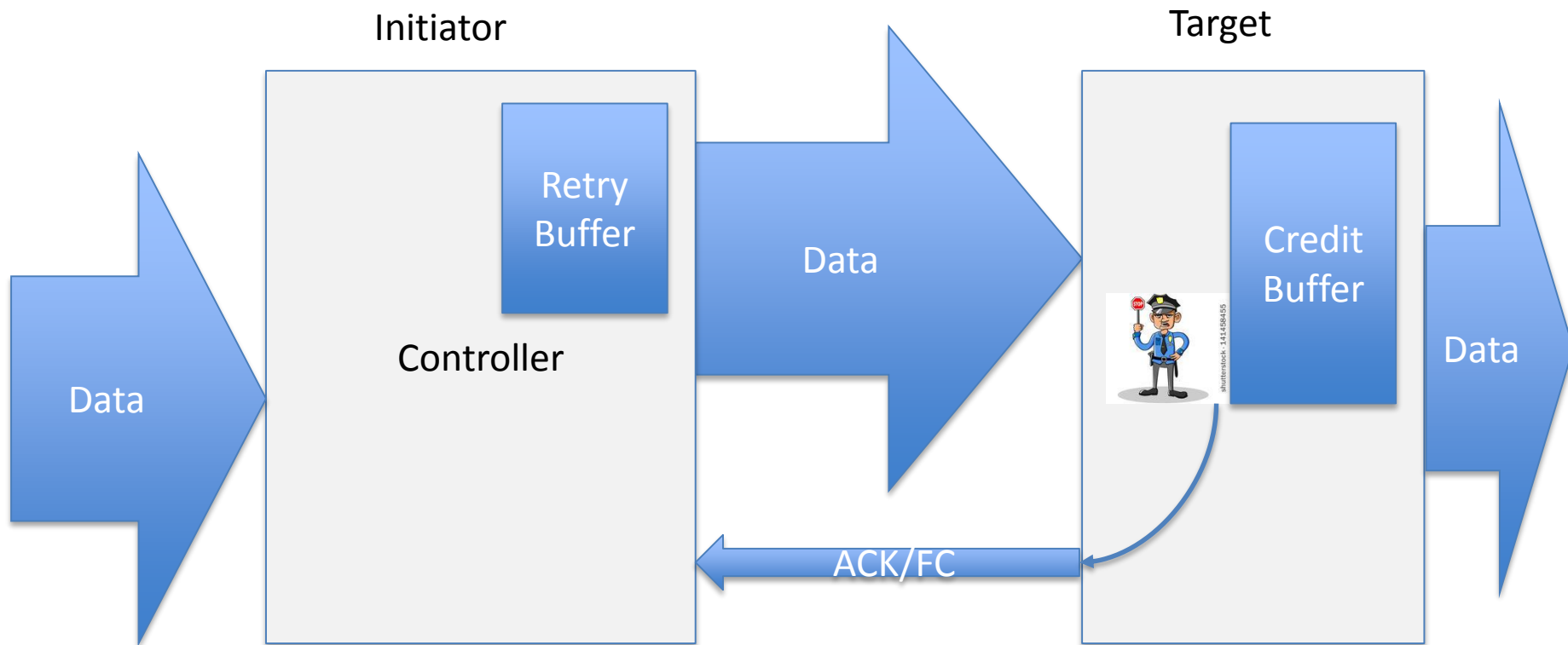


- **Stores TLPs Pending ACK**
- **Link Partner ACKS**
 - Required Limit on ACK Latency
- **Account for Latency**
 - Retimers
 - L0s exit
- **Implies RAM area**

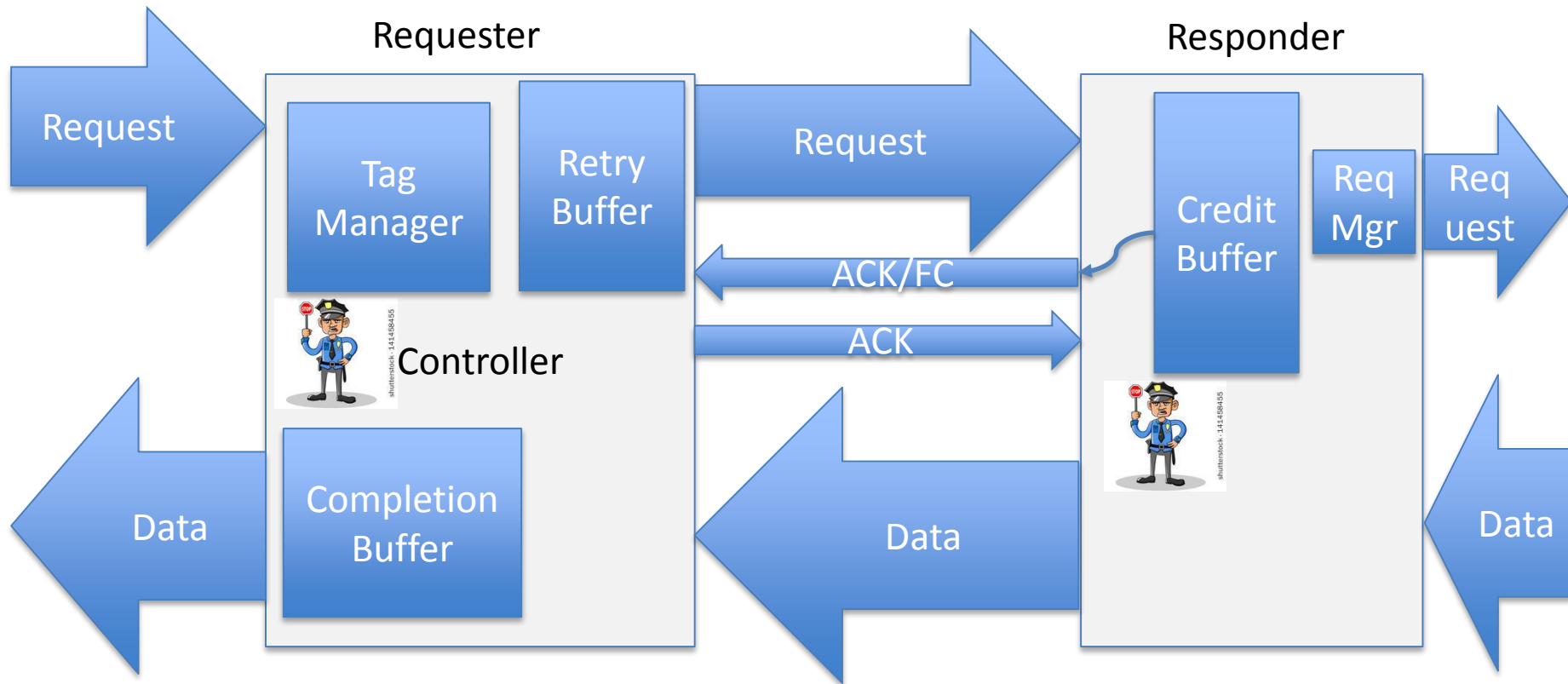


- **Defines Ability of a receiver to sink data**
- **Data Credit**
 - Stream between FC updates
- **Header**
 - Stream small packets
- **Posted/Non-Posted/Completions**
 - Most Important: P data credits, NP header credits
 - Least Important: NP data credits
 - Infinite Completion Credits

Pushing Data (Posted Requests)

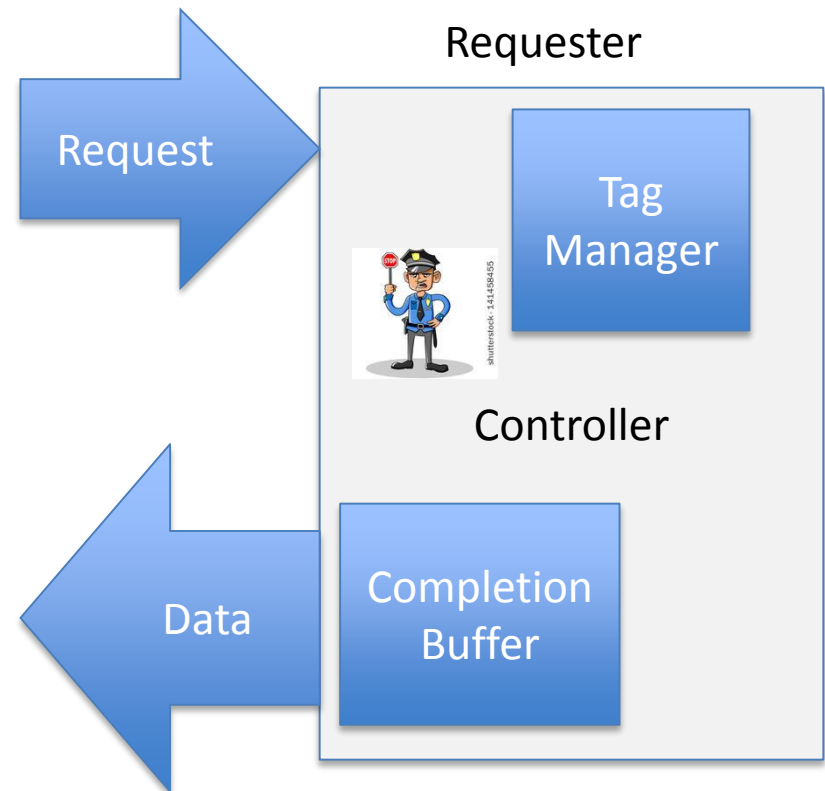


Pulling Data (NP Requests/Completions)



NP Requests - Requester

- **Requester wants data**
- **Needs a tag to associate data with a request**
- **Each Tag consumes resources – tracking logic + storage**
- **More Tags == performance**



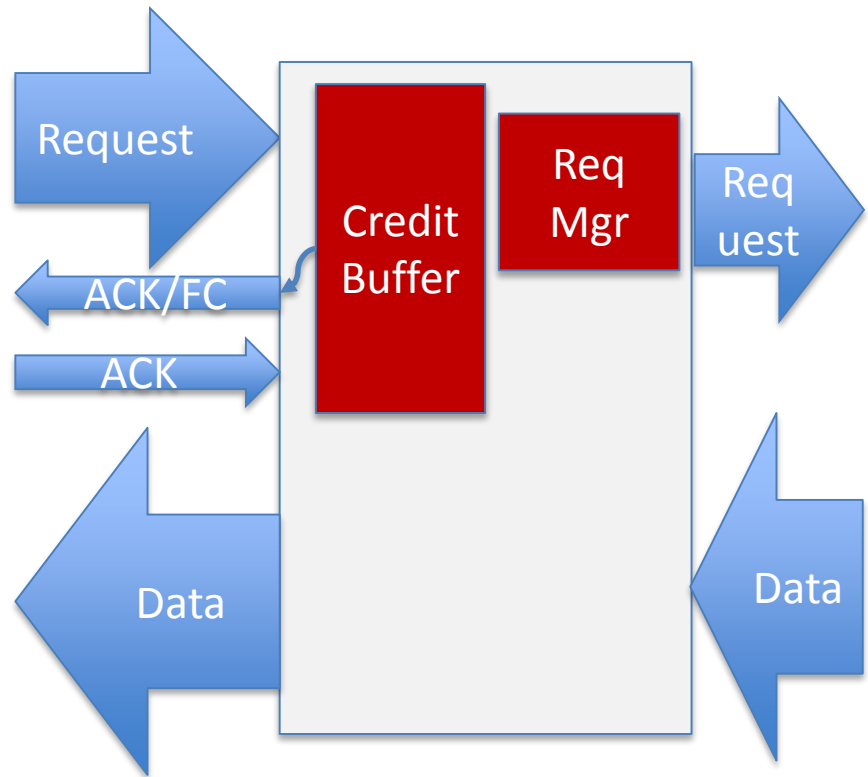
NP Requests – Transaction Sizes



- **Maximum Payload Size**
- **Maximum Read Request Size**
- **Multiple Completions**
- **Application Read Request Size**

NP Requests - Responder

- **Responder Manages Inbound Requests**
- **How many outstanding Requests to Support?**
- **Consider the Expected Round Trip Time**
- **How many NP FC credits to advertise?**

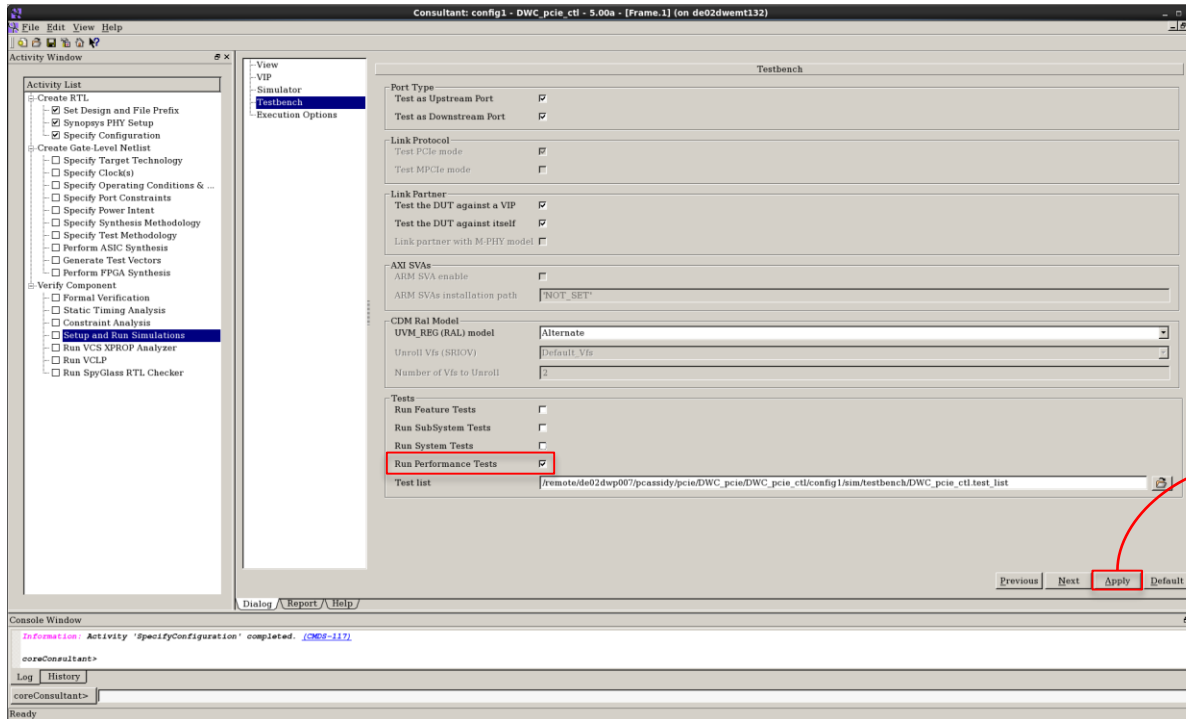


Performance Testing



- **A performance test suite allows trade offs to be analysed**
- **Real PHY model ensures FC/Ack Latencies are realistic**
- **Area vs. Performance decisions can be taken**

Performance Test Suite



Scenario: 00_MEM_00_MAX_00P												
PCIe Link Bandwidth												
Direction	Link	Total Transfer Size (Bytes)	Average Transfer Size (Bytes)	Traffic Bandwidth (G/s)	Data R/W (MB/s)	Link Loss (%)	Core Speed (G/s)	Core Loss (%)				
W0	GEN4 x16	65536	256.00	UPSTREAM: 0.008 DOWNSTREAM: 99.876 PCIe: 0.007	28.960	28.188	0.781	28.188	0.781			
T0	GEN4 x16	0	0	DOWNSTREAM: 0.007 UPSTREAM: 99.533	0.000	0.000	0	0.000	0			
Application Interface Bandwidth												
Interface	Clock Period (ns)	Total Transfer Size (Bytes)	Average Transfer Size (Bytes)	Transfer/Clock (Bytes/c)	Data R/W (MB/s)	Transfer/Device (ns)	Link Latency					
Client1	5	0	0	984.02	0.000	100.00	1.34					
AccessPort1	5	65536	256.00	13.322	28.065	99.58	0.05					
Link Latency												
PS	DLX	TL	Jitter (ns)		Total RX							
22	4	4	4	28	28							
AccessPort1	TL	DLX	PS		Total TX							
5	5	5	11		22							

- Allows Performance under various scenarios to be measured

Performance Test Suite



Scenario: OB_MEM_RD_MAX_CAP									
PCIe link Bandwidth									
Direction	Link	Total Transfer Size (bytes)	Average Transfer Size (bytes)	Traffic breakdown (%)	Data B/W (GB/s)	Link Ideal (GB/s)	Link Loss (%)	Core Ideal (GB/s)	Core Loss (%)
RX	GEN4 x16	65536	256.00	UPDATE_FC_NP: 0.068 Replays: 0 CPL_D/3DW/NO_ECRC: 99.876 ACK: 0.057	28.960	29.188	0.781	29.188	0.781
TX	GEN4 x16	0	0	Replays: 0 ACK: 0.467 MEM_RD/3DW/NO_ECRC: 99.533	0.000	0.000	0	0.000	0
Application Interface Bandwidth									
Interface	Clock Period (ns)	Total Transfer Size (bytes)	Average Transfer Size (bytes)	Transactions (Mxact/s)	Data B/W (GB/s)	Source Active (%)	Sink Pacing (%)		
Client1	1	0	0	984.62	0.000	100.00	1.54		
RADMTrgt1	1	65536	256.00	113.22	28.985	90.58	0.00		
Idle Latency									
PL	DLL	TL	rADM TRGT1	Total RX					
32	4	4	18	58					
xADM1	TL	DLL	PL	Total TX					
1	5	5	11	22					

- **Simulation Environment calculates performance for a given scenario**

Example X4 Link 2 Tags

Scenario: OB_MEM_RD_MAX_CAP

PCIe link Bandwidth

Direction	Link	Total Transfer Size (bytes)	Average Transfer Size (bytes)	Traffic breakdown (%)	Data B/W (GB/s)	Link Ideal (GB/s)	Link Loss (%)	Core Ideal (GB/s)	Core Loss (%)
RX	GEN4 x4	1048576	256.00	UPDATE_FC_NP: 1.992 Replays: 0 UPDATE_FC_P: 0.005 CPL_D/3DW/NO_ECRC: 96.199 ACK: 1.805	4.726	7.028	32.755	7.028	32.755
TX	GEN4 x4	0	0	UPDATE_FC_NP: 0.049 Replays: 0 UPDATE_FC_P: 0.049 ACK: 16.637 MEM_RD/3DW/NO_ECRC: 83.266	0.000	0.000	0	0.000	0

Application Interface Bandwidth

Interface	Clock Period (ns)	Total Transfer Size (bytes)	Average Transfer Size (bytes)	Transactions (Mxact/s)	Data B/W (GB/s)	Source Active (%)	Sink Pacing (%)
Client1	1	0	0	18.47	0.000	3.69	49.99
RADMCplBy	1	1048576	256.00	18.46	4.726	60.21	0.00

Idle Latency

PL	DLL	TL	rADM BYP	Total RX
31	3	5	2	41
xADM1	TL	DLL	PL	Total TX
2	3	5	12	22

Example X4 Link 128 Tags



Scenario: OB_MEM_RD_MAX_CAP

PCIe link Bandwidth

Direction	Link	Total Transfer Size (bytes)	Average Transfer Size (bytes)	Traffic breakdown (%)	Data B/W (GB/s)	Link Ideal (GB/s)	Link Loss (%)	Core Ideal (GB/s)	Core Loss (%)
RX	GEN4 x4	1048576	256.00	UPDATE_FC_NP: 1.465 Replays: 0 UPDATE_FC_P: 0.003 CPL_D/3DW/NO_ECRC: 97.225 ACK: 1.308	7.074	7.103	0.408	7.103	0.408
TX	GEN4 x4	0	0	UPDATE_FC_NP: 0.035 Replays: 0 UPDATE_FC_P: 0.035 ACK: 11.449 MEM_RD/3DW/NO_ECRC: 88.482	0.000	0.000	0	0.000	0

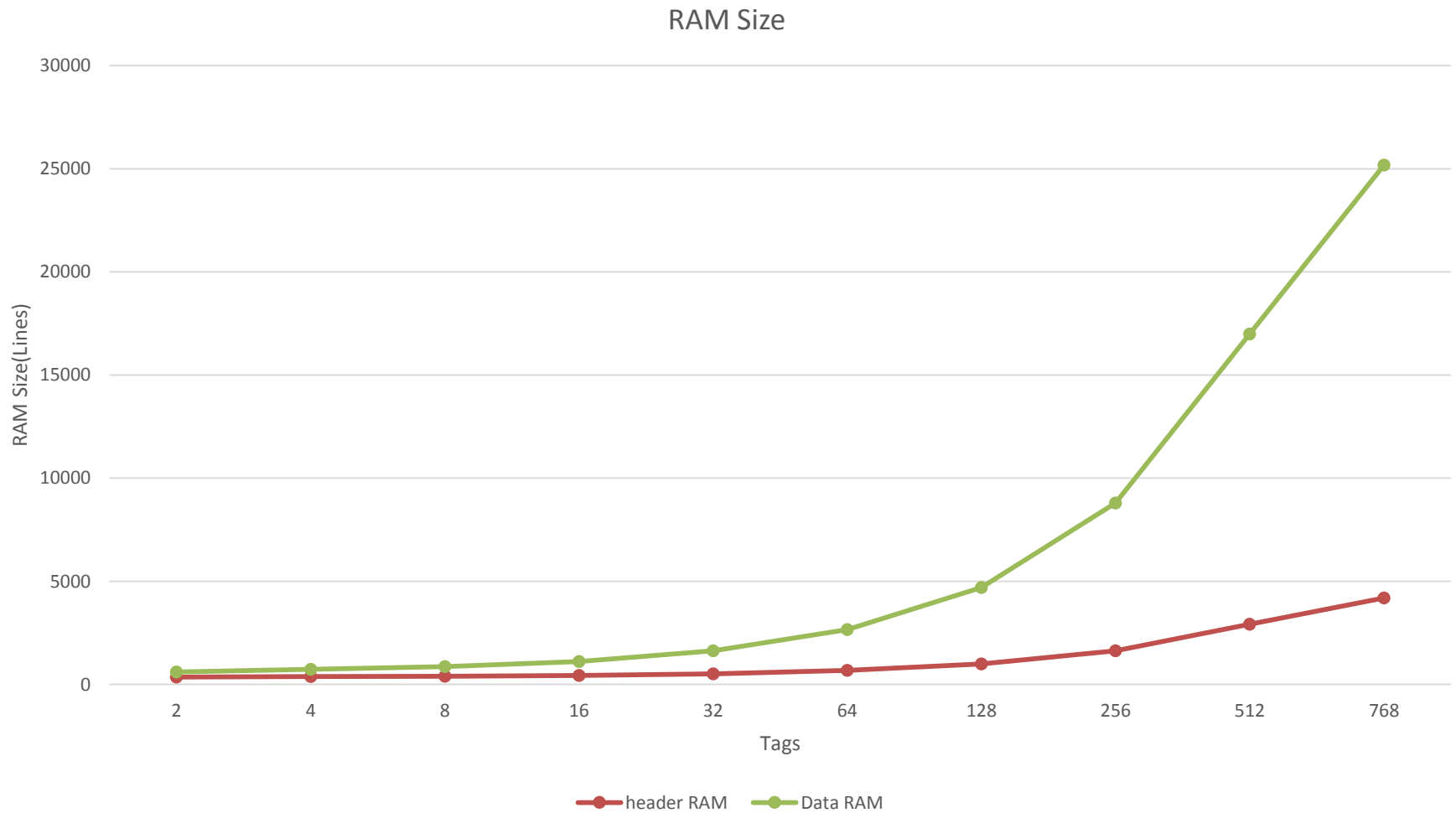
Application Interface Bandwidth

Interface	Clock Period (ns)	Total Transfer Size (bytes)	Average Transfer Size (bytes)	Transactions (Mxact/s)	Data B/W (GB/s)	Source Active (%)	Sink Pacing (%)
RADMTgt1	1	1048576	256.00	27.63	7.074	88.43	0.00
Client1	1	0	0	28.48	0.000	5.79	50.83

Idle Latency

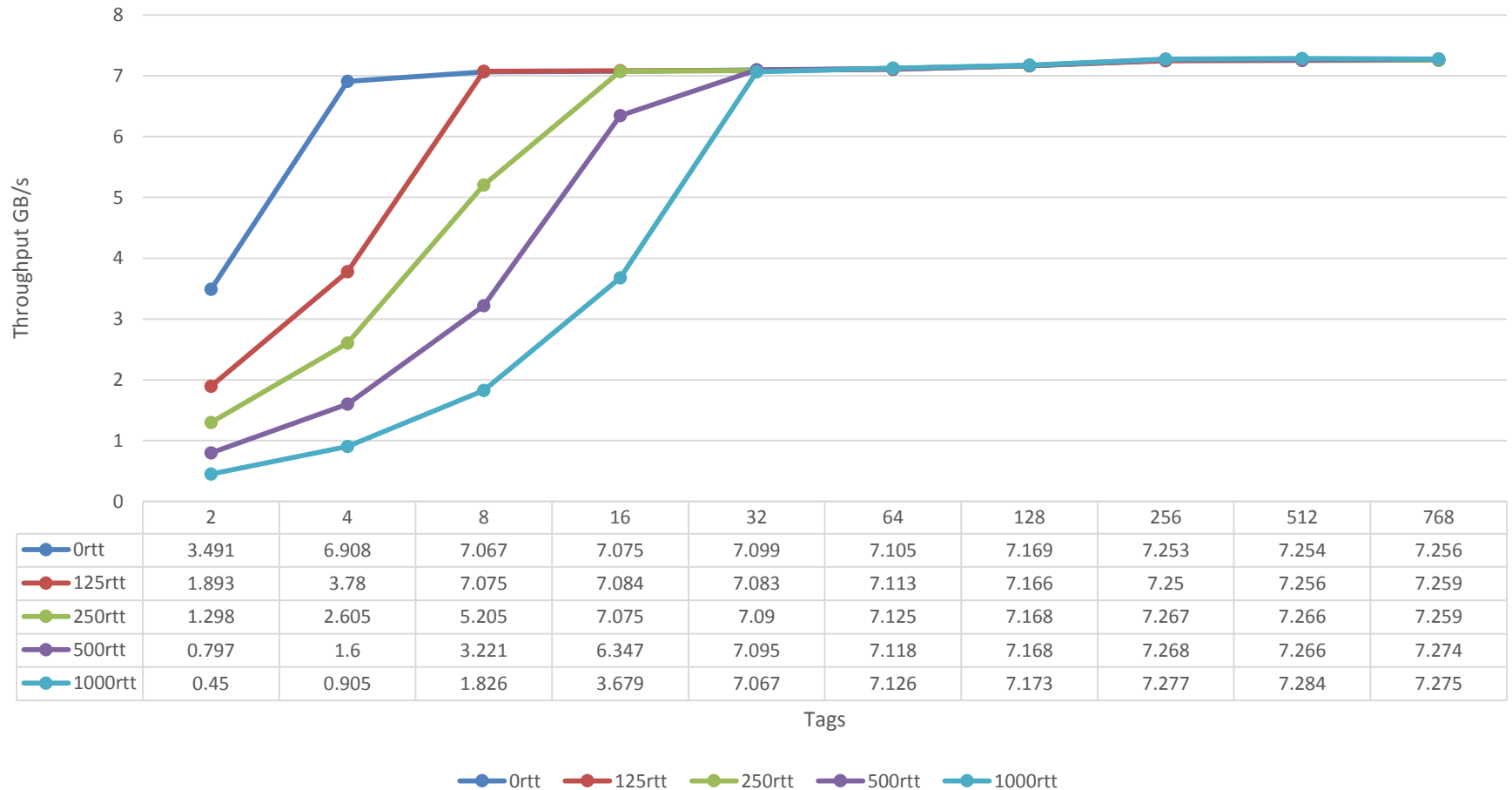
PL	DLL	TL	rADM TRGT1	Total RX
31	3	5	41	80
xADM1	TL	DLL	PL	Total TX
2	3	5	12	22

RAM vs. Tags



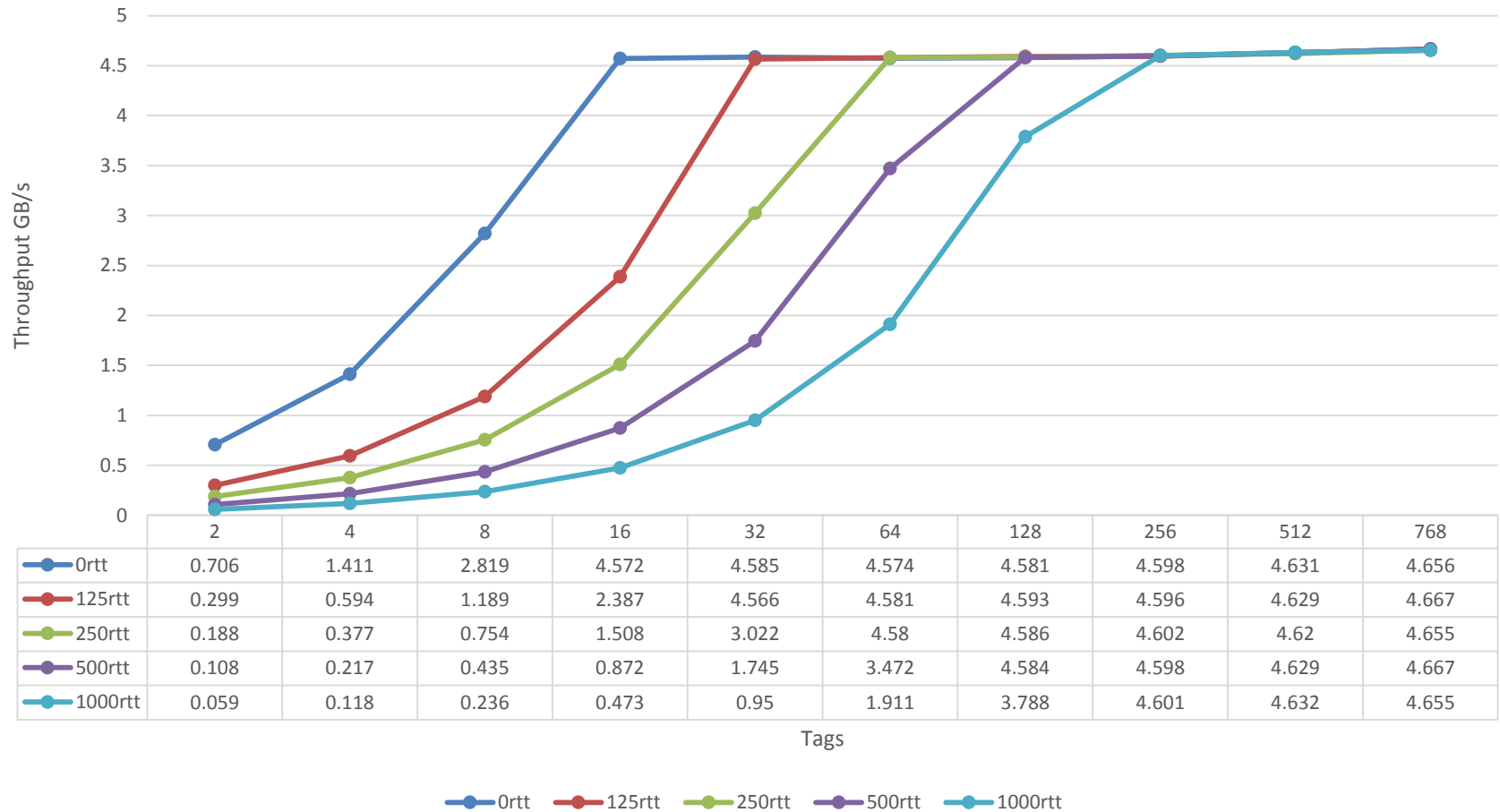
Tags vs. Performance X4

Simulation Results: 16 GT/s X4 256 Byte Request Size



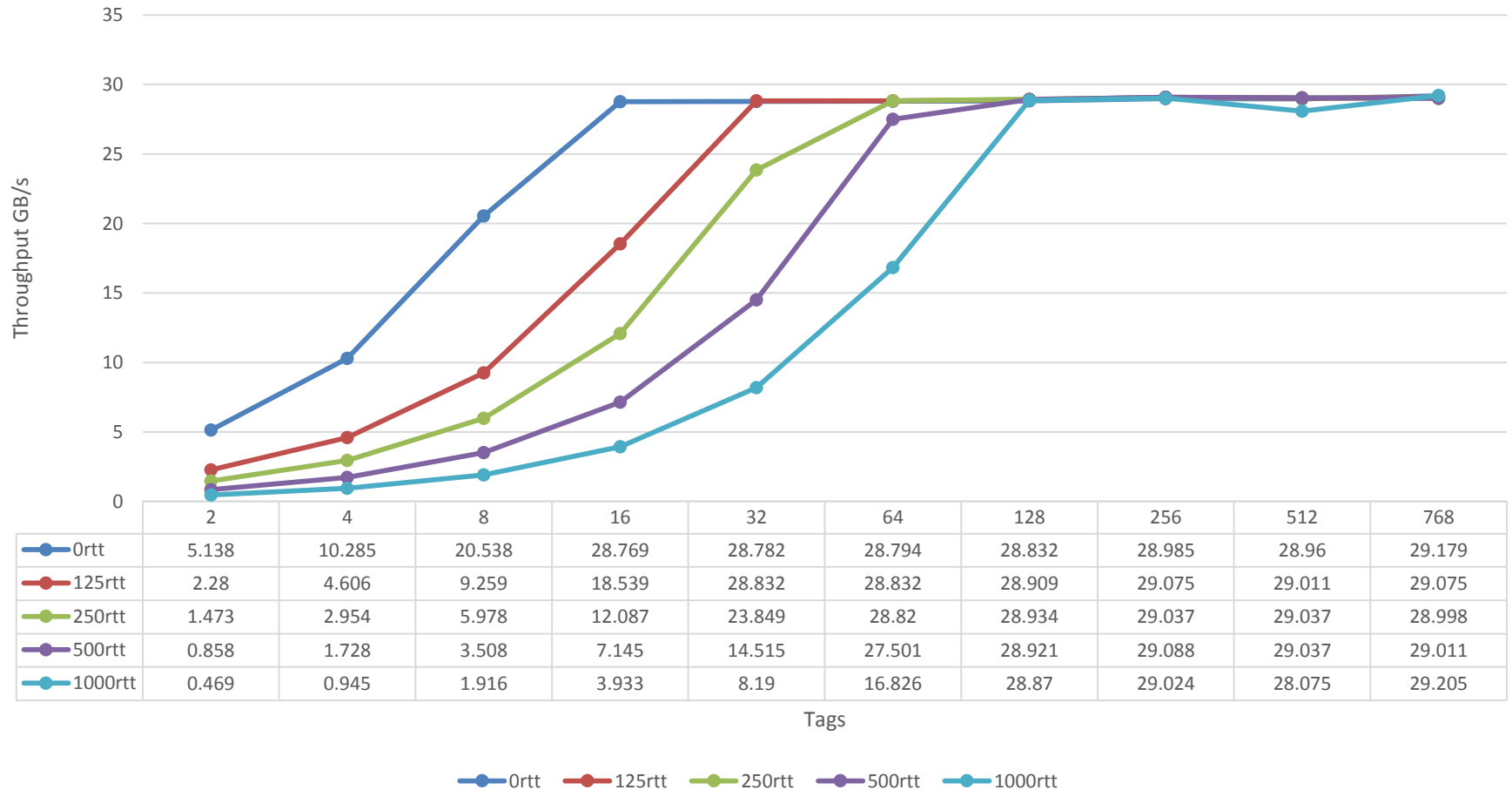
Tags vs. Performance X4

Simulation Results: 16 GT/s X4 32 Byte Request Size



Tags vs. Performance X16

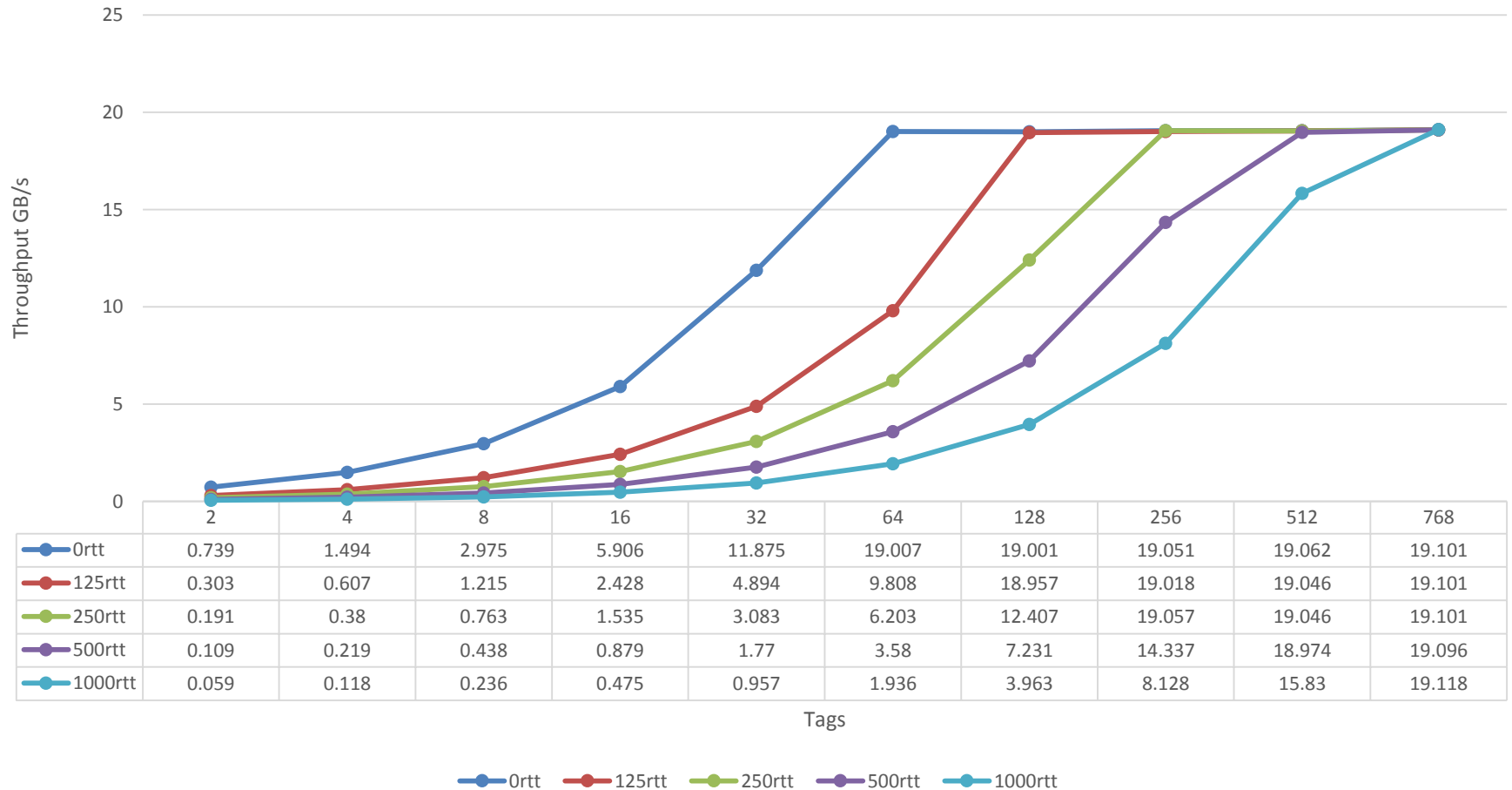
Simulation Results: 16 GT/s X16 256 Byte Request Size



Tags vs. Performance X16



Simulation Results: 16 GT/s X16 32 Byte Request Size



- **Trade Offs**
 - Look at number of credits advertised
 - Look at Tags in particular
 - Consider Round trip time
 - How much RAM/area can I afford

- **Use performance simulation to verify goals are met**

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